Appl. No. 10/715,611
Examiner: PHAM, THANHHA S, Art Unit 2813
In response to the Office Action dated August 23, 2005

Date: November 3, 2005
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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-19 (canceled)

Claim 20 (previously presented): A method of a filling bit line contact via, comprising:
providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;
forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region;
conformally forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region;
etching the doped conductive layer to leave a remaining portion of the doped conductive layer lower than the top surface of the gate electrode overlying the drain region;
conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and
forming a first conductive layer filling the bit line contact via and periphery contact via.